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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,001	08/04/2003	Ming-Ching Chang	67,200-1107	5032

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EXAMINER	
GEORGE, PATRICIA ANN	
ART UNIT	PAPER NUMBER
1765	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/634,001	CHANG ET AL.	
	Examiner	Art Unit	
	Patricia A. George	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/4/2007 has been entered. Amendments submitted 12/11/2006 will be address in the new grounds of rejection below.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim1-13 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant amended claim 1, to include a negative limitation "said plasma treatment performed without material deposition." Please see MPEP Section 2173.05 (i). "The mere absence of a positive recitation is not basis for an exclusion. Any claim containing a negative limitation which does not have basis in the

original disclosure should be rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3, 5-8, and 14-15, and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Westerheim et al. (High-density inductively coupled plasma etch of sub half micron critical layers: Transistor polysilicon gate definition and contact formation; American Vacuum Society Sept./Oct 1998, pg 2699-2706; Digital Semiconductor) (herein referred to as Westerheim) in view of Wang et al. (6,127,278), Khan et al. (2003/0003748), and Hwang et al. (Ion mass effect in plasma induced charging, June 1997; AIP).

Westerheim teaches a method for improving a polysilicon gate electrode profile, which includes the following steps. The last main step, overetch, includes two steps the first a treatment at higher wafer bias to maintain directionality during the transition from

the main etch, which helps to reduce transition effects such as notching at the base of the polysilicon line.10 Then, wafer bias is reduced for the longer second step to increase selectivity to oxide (see 4. Overetch). A semiconductor process wafer is provided which comprise gate oxide (i.e. dielectric) formed over a silicon substrate and a polysilicon layer formed over the gate dielectric (see Fig. 1). CD9 or CD11, a polyarylethersulfone anti-reflective coating (i.e. hardmask layer or ARC) is over the polysilicon layer(see Fig. 1, and section 2.ARC defectivity). The ARC is patterned for forming a gate electrode by using a patterned resist (i.e. according to a photolithographic patterning process) (see introduction). A first reaction ion etch (RIE) step is used to etch through a thickness of the hardmask layer to expose the polysilicon layer (see Introduction). A second RIE step is used to etch (breakthrough) a first thickness portion of the polysilicon layer (see Introduction) including moderate RF source and bias power (see B. Tool description and 2. Initiation Etch). A third RIE step is used to etch through a second thickness portion of the polysilicon layer to expose portions of the underlying gate dielectric (see 3. Main Etch). Westerheim teaches the next main etch step, overetch, included two steps: first a plasma process (i.e. treatment) that exposes the polysilicon layer in-situ using an HDP system with a relatively low wafer bias voltage (i.e. to neutralize an electrical charge imbalance – see top of second col. of first page) without material layer deposition – to remove the notch, and then a final (or fourth) RIE overetch process, used to remove the remaining portion of polysilicon (see 4. Overetch). Examiner select the first sub-step of Westerheim's fourth

main process titled Overetch, as applicant's designated treatment step, and the second sub-step as applicants' designated overetch step.

Although Westerheim calls the Last RIE step of overetch one of four main steps, it would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the invention of etching polysilicon gates, as Westerheim, to include the two substeps of the overetch includes steps of treatments and overetching, as applicants claim, because the term treat means to subject to a process, action, or change, and Westerheim's steps of Overetch remove residual polysilicon, which result in either of the two steps being a step of treatment and/or overetch. For the sake of examination the first sub-step in the main Overetch process will be refered to as the treatment and the second sub-step in the main Overetch process will be refered to as the overetch.

Westerheim fails to teach the 3rd step (polysilicon main etch) is at least one of a lower RF source power and RF bias power compared to the 2nd (initial polysilicon etch) step, as in claims 1, 5, and 14, and 15.

Wang et al. (6,127,278) teaches the main etch steps of silicon containing materials, typically require less rf power (bias and coil (i.e. source)) as etching continues in order to obtain etched openings that are more perpendicular to the surface of the substrate (see col.4, lines 25-32, and col. 5 lines 28-31).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the invention of forming polysilicon gates, as

Westerheim, to include that 3rd step (polysilicon main etch) has lower RF bias power compared to the 2nd (initial polysilicon etch) step, as applicant claims, because Wang et al. teaches the forming of a desirable structure (one with openings that are more perpendicular to the surface of the substrate) results from etching silicon containing films in a manner which uses less rf bias as etching steps continue. In absence of unexpected results it would be obvious to select any value of rf bias which resulted in desirable results.

Westerheim is silent as to the use of an inert gas with the step of plasma treatment, as in claims 1 and 14.

Hwang et al. teaches inert gas is used in overetch (i.e. treatment) steps to improve plasma stability and facilitate profile control (see introduction, para. 1).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include use of an inert gas with the overetch step of plasma treatment, when modifying the invention of etching polysilicon gates, as Westerheim, because Hwang et al. teaches use of inert gas in such steps improves plasma stability and facilitate profile control.

As to claims 2, 3, and 14, Westerheim fails to teach the step of overetch, applicants' fourth step, is without RF bias.

Khan et al. teaches, in para. 5, a method for eliminating notches at the interface of silicon and an insulator, which includes the step of overetch carried out without bias power (see background and page 3, line starting "7.").

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the invention of etching silicon at the insulator interface, as Westerheim, to include a step of overetch which is carried out without bias power, as Khan et al., because Khan et al. teaches the step is carried out to remove debris from the bottom of the opening, such as notching.

As to claims 6 and 16, Hwang et al. teaches inert gas, such as Helium is used in overetch (i.e. treatment) steps to improve plasma stability and facilitate profile control (see introduction, para. 1).

As to claims 7 and 8, Westerheim teaches the fourth RIE etch (the overetch) is carried out with a chlorine-free etching chemistry comprising HBr and oxygen (see section 4. Overetch).

Claim Rejections - 35 USC § 103

Claim 4, 9, 11-12, 17-19, and 21-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Westerheim et al., Wang et al., Khan et al.. and Hwang et al. in view of Lee of USPN 5,665,203

The modified invention of Lee fails to teach the limitations of claim 4.

As for claim 4, Lee illustrates in figure 2 (parts 28 and 30) that the polysilicon layer includes both n and p doped regions used to form doped polysilicon gate electrodes shown in parallel (col.3, l.42-46).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the invention of forming polysilicon gate electrodes, as Westerheim, to include the polysilicon layer includes both n and p doped regions used to form doped polysilicon gate electrodes, because Lee teaches it is well known and function to form devices in this manner. It has been held that use of known and effective methods of manufacturing are cost saving.

As for claims 9 and 19, Lee discloses a combination of HBr/Cl.sub.2/O.sub.2 in the first and second etch steps (col.4, l.39-40 and c.4, l.46-50).

As for claims 11 and 21, Lee discloses the gate dielectric is thermally grown SiO.sub.2 (col.3, l.33-34).

As for claims 12 and 22, Lee discloses hardmask layers are made of LTO (col.3, l53 and 55).

Claim Rejections - 35 USC § 103

Claims 10, 13, 20, and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Westerheim et al., Wang et al., Khan et al.. and Hwang et al. in view of Lill et al. of USPN 6,284,665.

The modified invention of Westerheim et al. fails to teach the limitations of claims 10, 13, 20, and 23.

Lill et al. teaches typical process conditions for RIE of polysilicon. Lill teaches the use of no-bias power to minimize the amount of self-bias on the substrate (col.10, l.15-30), as in claims 13, and 23. Lill also teaches the RF bias power is supplied at the claimed frequency of greater than about 1 MHz (col.8, l.4) and in figure 2 Lill illustrates the RF bias power and is adjustably decoupled (col.10, l.4) from the RF source power, as in claims 10 and 20.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to use the typical process conditions for RIE of polysilicon selectively to silicon nitride, of Lill, when using the method of RIE for polysilicon gate structures, of Lee, because Lill teaches they are typical and effective for RIE of polysilicon. It have been held that use of methods known to be typically effective is a cost savings.

Claim Rejections - 35 USC § 103

Claims 10, 13, 20, and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Westerheim et al., Wang et al., Khan et al.. and Hwang et al. in view of Wolf et al (Silicon Processing for the VLSI Era; Vol. 1; 1986; Lattice Press) .

The modified invention of Westerheim et al. fails to teach the limitations of claims 10, 13, 20, and 23.

Wolf teaches rf source and bias powers, as well as the rf frequency are process parameters which can be determined through factorial experimental design. (See p.546-547, and 618).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the method of etching polysilicon, of Lee, to include process parameters such as rf source and bias powers and frequency, can be determined by one skilled in the art through factorial experiemental design, as Wolf, because Wolf teaches settings for excitation powers and frequencies are parameters in plasma process known to be derived and controlled by one skilled in the art, derived by such statistical experimentation.

Response to Arguments

Applicant's arguments, see remarks, filed 11/12/2006, with respect to the rejection(s) of claim(s) 1-23 have been fully considered.

Applicant's arguments, on page 17, about the formation of nitride layers by the plasma treatment step of Nallan et al. (prior to etching the gate dielectric) in Lee et al., would form nitride layers on the gate dielectric and over the sidewall oxide residues of Lee, thus interfering with the subsequent HF dip, toward claim 1 are persuasive, therefore, a new grounds of rejection has been offered above.

Applicants' make several remarks throughout the response as to how prior art references the step number, as apposed to how examiner number the step number.

Examiner interpret the term step as meaning any stage in a process, such as a sub-step of a main process, or a main process, each and all a step.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wolf et al (Silicon Processing for the VLSI Era; Vol. 1; 1986; Lattice Press). The reference of Wolf applies to all process parameters which could be determined through routine statistical experimentation. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571) 272-5955. The examiner can normally be reached on Tues. - Sat. between 8:00 am and 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Patricia A George
Examiner
Art Unit 1765

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NADINE G. NORTON
SUPERVISORY PATENT EXAMINER